

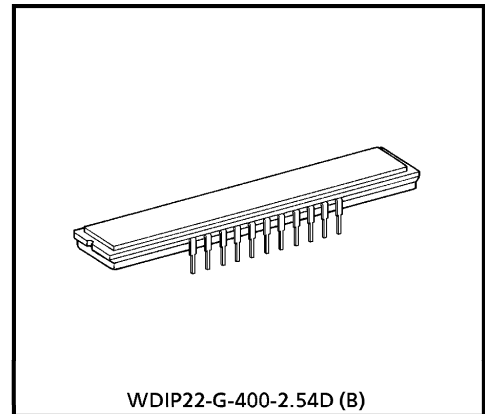
TOSHIBA CCD LINEAR IMAGE SENSOR CCD (Charge Coupled Device)

TCD1501D

The TCD1501D which includes sample-and-hold circuit is a high sensitive and low dark current 5000 elements CCD image sensor.

The sensor is designed for facsimile, imagescanner and OCR.

The device contains a row of 5000 elements photodiodes which provide a 16 lines/mm (400DPI) across a A3 size paper. The device is operated by 5 V (pulse), and 12 V power supply.



Weight : 5.2 g (Typ.)

FEATURES

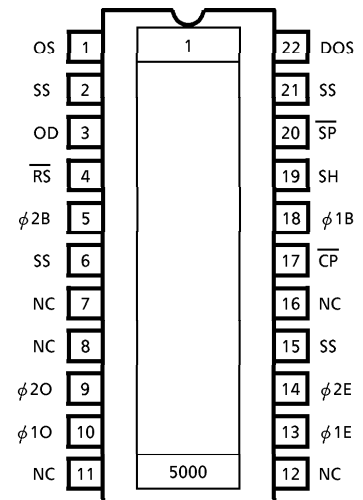
- Number of Image Sensing Elements : 5000 elements
- Image Sensing Element Size : 7 μm by 7 μm on 7 μm centers
- Photo Sensing Region : High sensitive and low voltage dark signal pn photodiode
- Clock : 2 Phase (5 V)
- Internal Circuit : S / H circuit
- Package : 22 pin Cerdip

MAXIMUM RATINGS (Note 1)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|-------------------------------|------------|----------|------|
| Clock Pulse Voltage | V_{ϕ} | - 0.3~8 | V |
| Shift Pulse Voltage | V_{SH} | | |
| Reset Pulse Voltage | V_{RS} | | |
| Clamp Pulse Voltage | V_{CP} | | |
| Sample and Hold Pulse Voltage | V_{SP} | | |
| Power Supply Voltage | V_{OD} | - 0.3~15 | |
| Operating Temperature | T_{opr} | - 25~60 | °C |
| Storage Temperature | T_{stg} | - 40~100 | °C |

(Note 1) : All voltage are with respect to SS terminals (Ground).

PIN CONNECTIONS

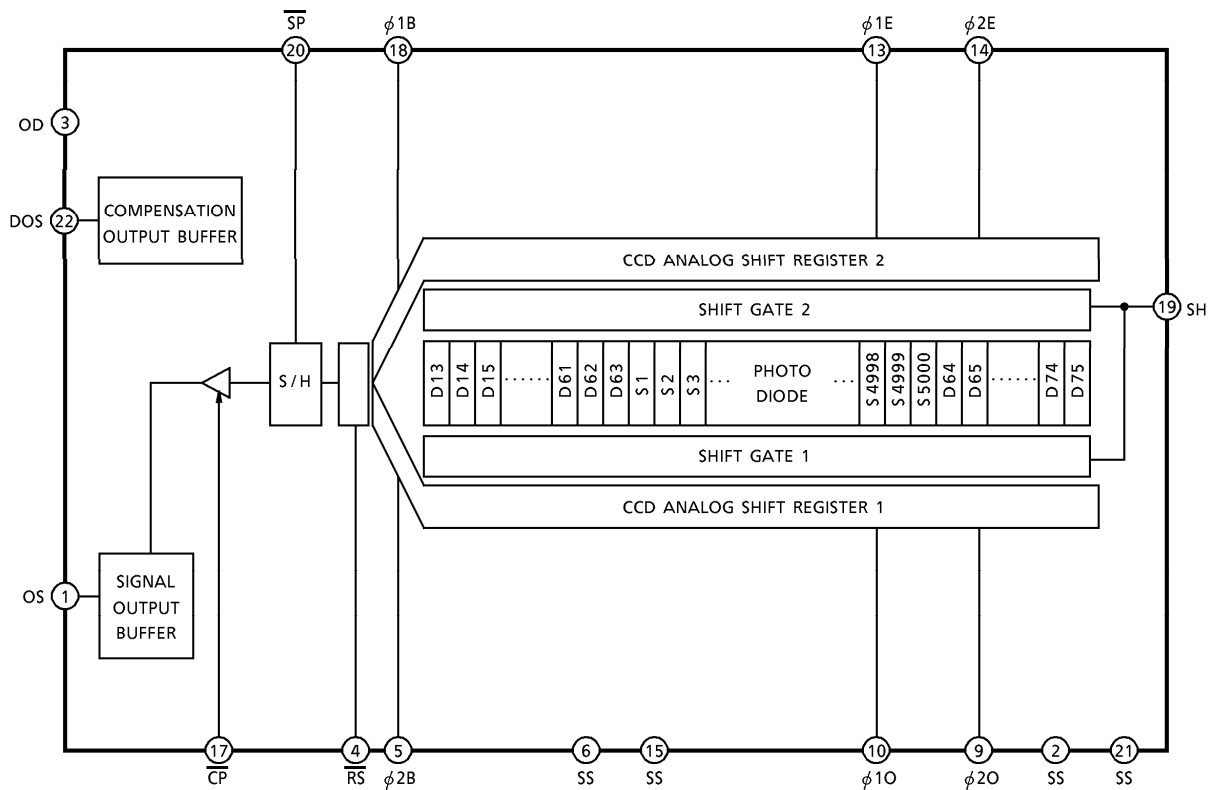


(TOP VIEW)

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CIRCUIT DIAGRAM



PIN NAME

| | |
|-----------------|-----------------------------|
| $\phi 1E, O$ | Clock (Phase 1) |
| $\phi 2E, O$ | Clock (Phase 2) |
| $\phi 1B$ | Final Stage Clock (Phase 1) |
| $\phi 2B$ | Final Stage Clock (Phase 2) |
| SH | Shift Gate |
| \overline{RS} | Reset Gate |
| \overline{SP} | Sample and Hold Gate |
| \overline{CP} | Clamp Gate |
| OS | Signal Output |
| DOS | Compensation Output |
| OD | Power |
| SS | Ground |
| NC | Non Connection |

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{OD} = 12 V, V_φ = V_{RS} = V_{SH} = V_{SP} = V_{CP} = 5 V, f_φ = 0.5 MHz, f_{RS} = 1 MHz, t_{INT} (INTEGRATION TIME) = 10 ms, LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP, LOAD RESISTANCE = 100 kΩ)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|--------------------------------|-----------------------------------|------|------|------|----------|----------|
| Sensitivity | R | 10.4 | 13 | 15.6 | V / lx·s | |
| Photo Response Non Uniformity | PRNU | — | — | 10 | % | (Note 2) |
| | PRNU (3) | — | 6 | 10 | mV | (Note 9) |
| Register Imbalance | RI | — | — | 3 | % | (Note 3) |
| Saturation Output Voltage | V _{SAT} | 2 | 3 | — | V | (Note 4) |
| Saturation Exposure | SE | 0.13 | 0.23 | — | lx·s | (Note 5) |
| Dark Signal Voltage | V _{DRK} | — | 1 | 2 | mV | (Note 6) |
| Dark Signal Non Uniformity | DSNU | — | 2 | 3 | mV | (Note 6) |
| DC Power Dissipation | P _D | — | 240 | 325 | mW | |
| Total Transfer Efficiency | TTE | 92 | — | — | % | |
| Output Impedance | Z _O | — | 0.5 | 1 | kΩ | |
| Dynamic Range | DR | — | 3000 | — | — | (Note 7) |
| DC Signal Output Voltage | V _{OS} | 4 | 5 | 6.5 | V | (Note 8) |
| DC Compensation Output Voltage | V _{DOS} | 4 | 5 | 6.5 | V | (Note 8) |
| DC Differential Error Voltage | V _{OS} -V _{DOS} | — | — | 400 | mV | |

(Note 2) : Measured at 50% of SE (Typ.)

$$\text{Definition of PRNU : PRNU} = \frac{\Delta\bar{x}}{\bar{x}} \times 100 (\%)$$

Where \bar{x} is average of total signal output and $\Delta\bar{x}$ is the maximum deviation from \bar{x} under uniform illumination.

(Note 3) : Measured at 50% of SE (Typ.)

RI is defined as follows:

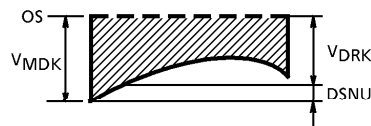
$$\text{RI} = \frac{\sum_{n=1}^{4999} |\chi_n - \chi_{n+1}|}{4999 \times \bar{x}} \times 100 (\%)$$

Where χ_n and χ_{n+1} are signal output of each pixel. \bar{x} is average of total signal output.

(Note 4) : V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

(Note 5) : Definition of SE : $SE = \frac{VSAT}{R} (I \times s)$

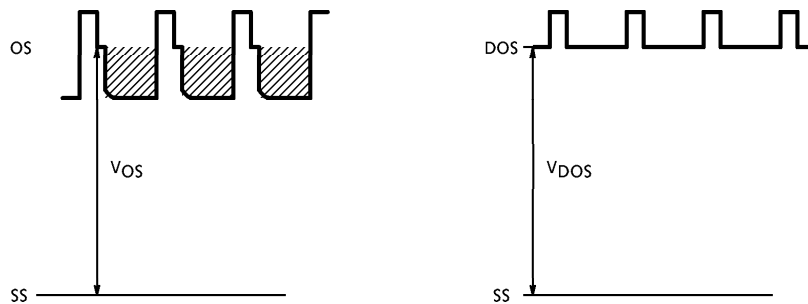
(Note 6) : V_{DRK} is defined as average dark signal voltage of all effective pixels.
 $DSNU$ is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



(Note 7) : Definition of DR : $DR = \frac{VSAT}{V_{DRK}}$

V_{DRK} is proportional to t_{INT} (Integration Time).
 So the shorter t_{INT} condition makes wider DR values.

(Note 8) : DC signal output voltage and DC compensation output voltage are defined as follows:



(Note 9) : PRUN (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.).

OPERATING CONDITION

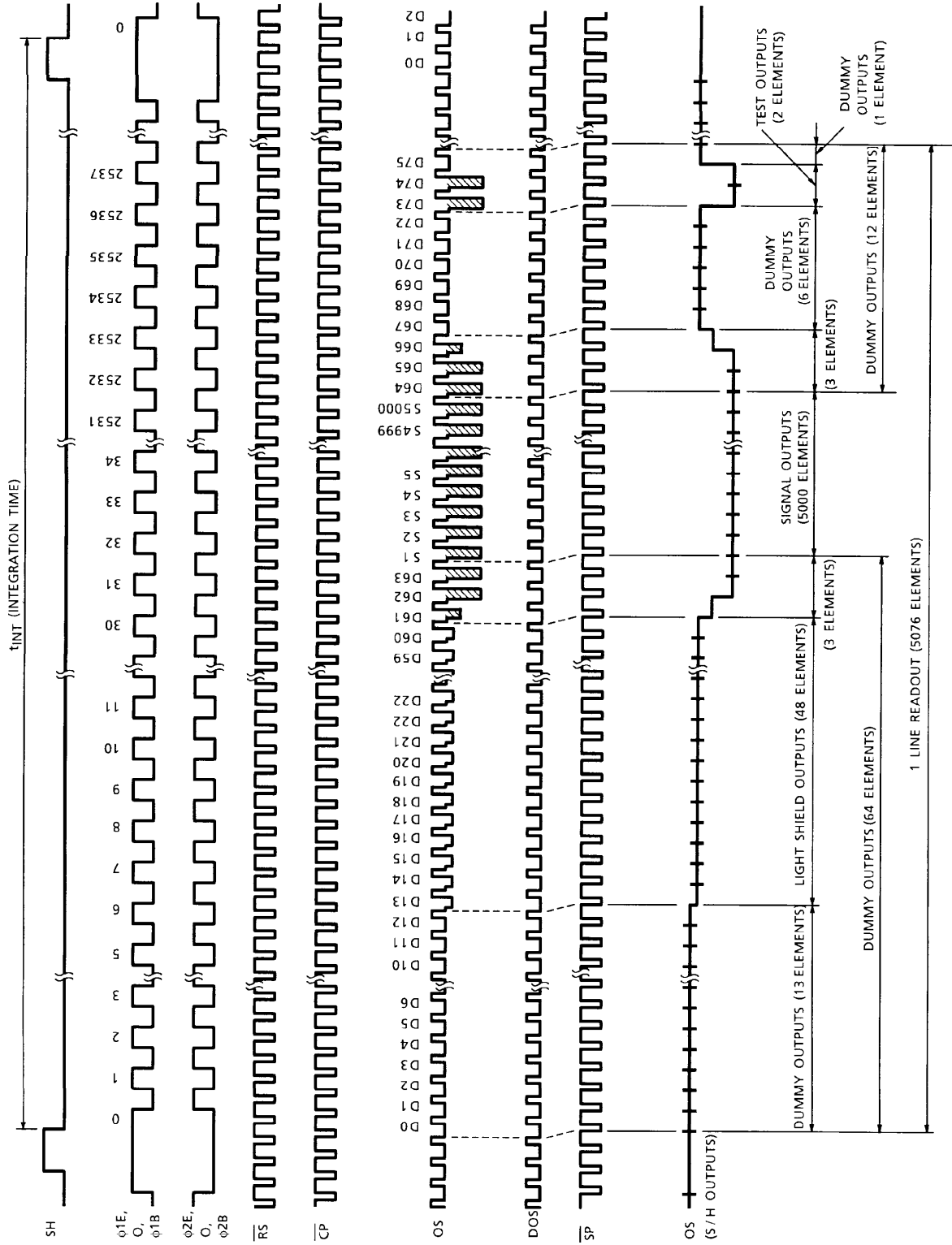
| CHARACTERISTIC | | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---------------------------------|-----------|------------------|------|------|------|------|
| Clock Pulse Voltage | "H" Level | $V_{\phi 1E, O}$ | 4.5 | 5 | 5.5 | V |
| | "L" Level | $V_{\phi 2E, O}$ | 0 | — | 0.5 | |
| Final Stage Clock Voltage | "H" Level | $V_{\phi 1B}$ | 4.5 | 5 | 5.5 | V |
| | "L" Level | $V_{\phi 2B}$ | 0 | — | 0.5 | |
| Shift Pulse Voltage | "H" Level | V_{SH} | 4.5 | 5 | 5.5 | V |
| | "L" Level | | 0 | — | 0.5 | |
| Reset Pulse Voltage | "H" Level | V_{RS} | 4.5 | 5 | 5.5 | V |
| | "L" Level | | 0 | — | 0.5 | |
| Clamp Pulse Voltage | "H" Level | V_{CP} | 4.5 | 5 | 5.5 | V |
| | "L" Level | | 0 | — | 0.5 | |
| Sample and Hold Pulse Voltage * | "H" Level | V_{SP} | 4.5 | 5 | 5.5 | V |
| | "L" Level | | 0 | — | 0.5 | |
| Power Supply Voltage | | V_{OD} | 11.4 | 12.0 | 13.0 | V |

* : Supply "L" level to \overline{SP} terminal when sample-and-hold circuitry is not used.

CLOCK CHARACTERISTICS (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|----------------------------------|---------------------|------|------|------|------|
| Clock Pulse Frequency | f_{ϕ} | — | 0.5 | 6.0 | MHz |
| Reset Pulse Frequency | $f_{\overline{RS}}$ | — | 1.0 | 12.0 | MHz |
| Sample and Hold Pulse Frequency | $f_{\overline{SP}}$ | — | 1.0 | 2.0 | MHz |
| Clock Capacitance | $C_{\phi E}$ | — | 350 | 450 | pF |
| | $C_{\phi O}$ | — | 350 | 450 | |
| Final Stage Clock Capacitance | $C_{\phi B}$ | — | 10 | 20 | pF |
| Shift Gate Capacitance | C_{SH} | — | 10 | 20 | pF |
| Reset Gate Capacitance | $C_{\overline{RS}}$ | — | 10 | 20 | pF |
| Clamp Gate Capacitance | C_{CP} | — | 10 | 20 | pF |
| Sample and Hold Gate Capacitance | $C_{\overline{SP}}$ | — | 10 | 20 | pF |

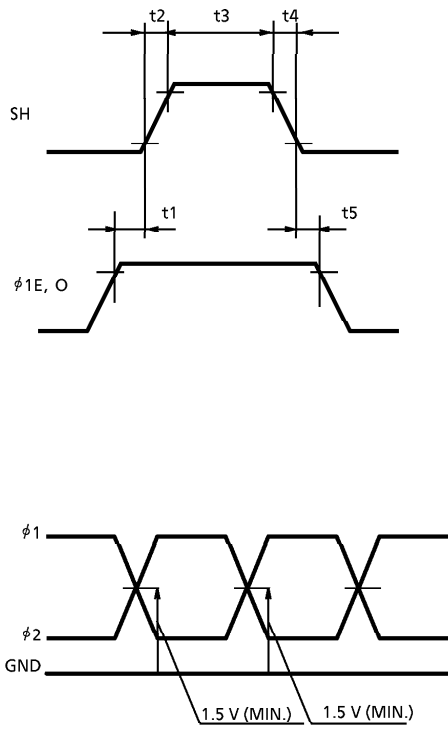
TIMING CHART



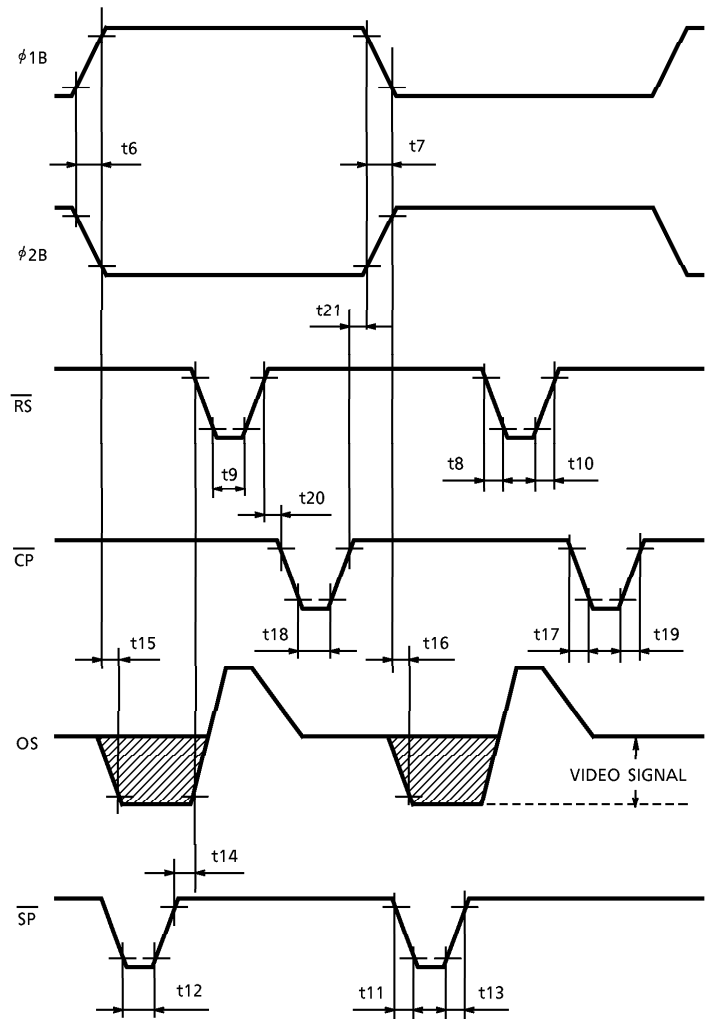
TCD1501D-6

TIMING REQUIREMENTS

SH, $\phi 1$ TIMING



$\phi 1, \phi 2, \overline{RS}, \overline{CP}, OS, \overline{SP}$ TIMING

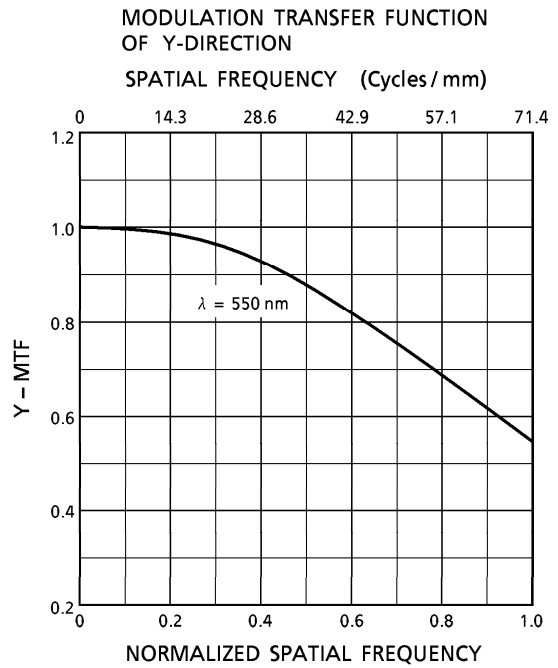
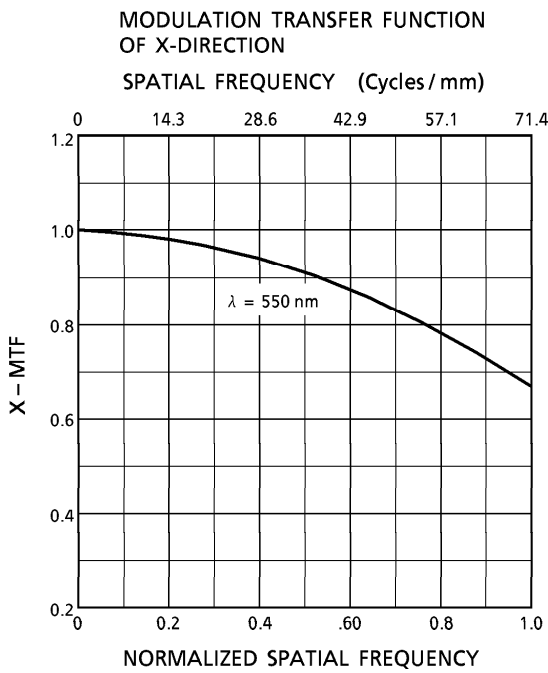
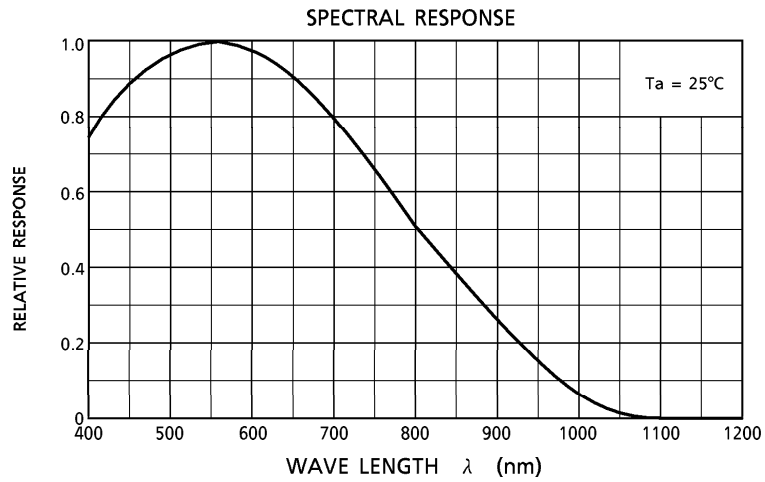


| CHARACTERISTIC | SYMBOL | MIN. | TYP. (Note 10) | MAX. | UNIT |
|--|----------|------|-------------------|------|------|
| Pulse Timing of SH and $\phi 10, E$ | t1, t5 | 100 | 300 | — | ns |
| SH Pulse Rise Time, Fall Time | t2, t4 | 0 | 50 | — | ns |
| SH Pulse Width | t3 | 500 | 1000 | — | ns |
| $\phi 1, \phi 2$ Pulse Rise Time, Fall Time | t6, t7 | 0 | 100 | — | ns |
| \overline{RS} Pulse Rise Time, Fall Time | t8, t10 | 0 | 20 | — | ns |
| \overline{RS} Pulse Width | t9 | 20 | 250 | — | ns |
| \overline{SP} Pulse Rise Time, Fall Time | t11, t13 | 0 | 20 | — | ns |
| \overline{SP} Pulse Width | t12 | 20 | — | — | ns |
| Pulse Timing of \overline{SP} and \overline{RS} | t14 | 0 | 50 | — | ns |
| Video Data Delay Time (Note 11) | t15, t16 | — | 30 | — | ns |
| \overline{CP} Pulse Rise Time, Fall Time | t17, t19 | 0 | 20 | — | ns |
| \overline{CP} Pulse Width | t18 | 20 | — | — | ns |
| Pulse Timing of \overline{RS} and \overline{CP} | t20 | 0 | — | — | ns |
| Pulse Timing of $\phi 1B, \phi 2B$ and \overline{CP} | t21 | 0 | — | — | ns |

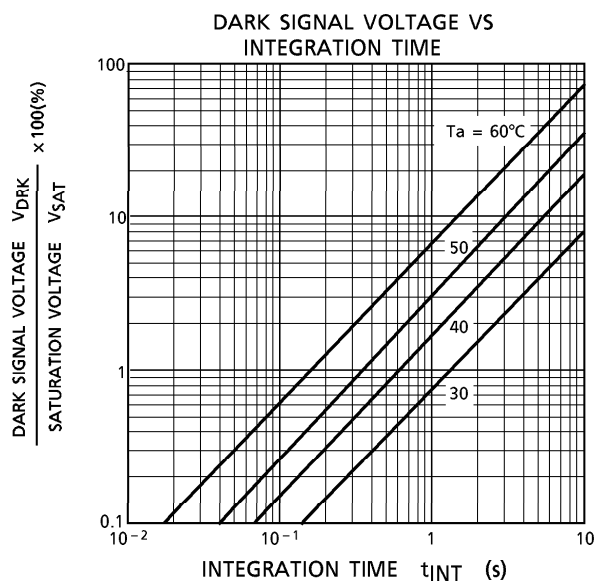
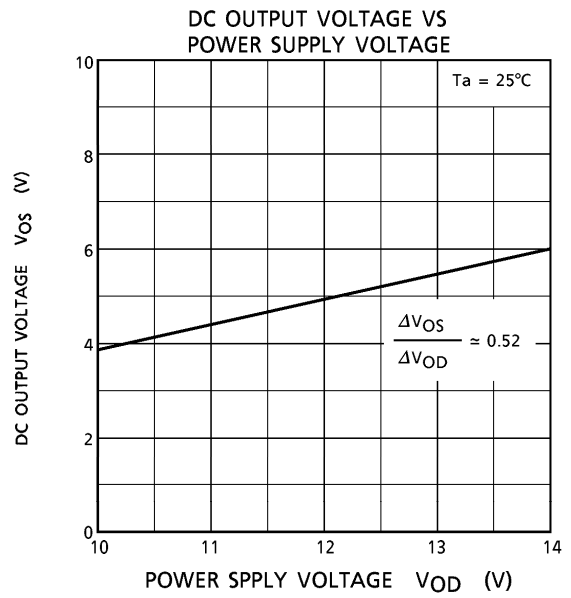
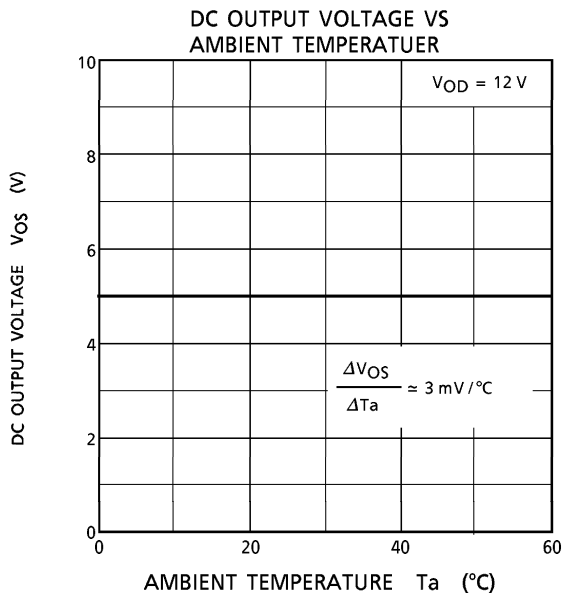
(Note 10) : TYP. is the case of $f_{RS} = 1.0$ MHz

(Note 11) : Load Resistance is 100 k Ω

TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES (Cont'd)



PRECAUTIONS FOR USE OF CCD IMAGE SENSOR**1. Static Electricity**

This device has some weakly terminals for static electricity. Therefore, please pay attention to treat this device.

CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting plier or pincette.

It is not necessarily required to execute all precaution items for static electricity.

It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2 Window Glass

As the dust and station on the glass window of the package will cause black flow on the picture, never fail to clean the glass surface before using. (Blow compressed vapor, and wipe off the dust, and dirt with soft cloth or paper slightly moistened with alcohol).

Fully take care for the handling of the device as the window glass will break or a strong friction is given to the window glass surface.

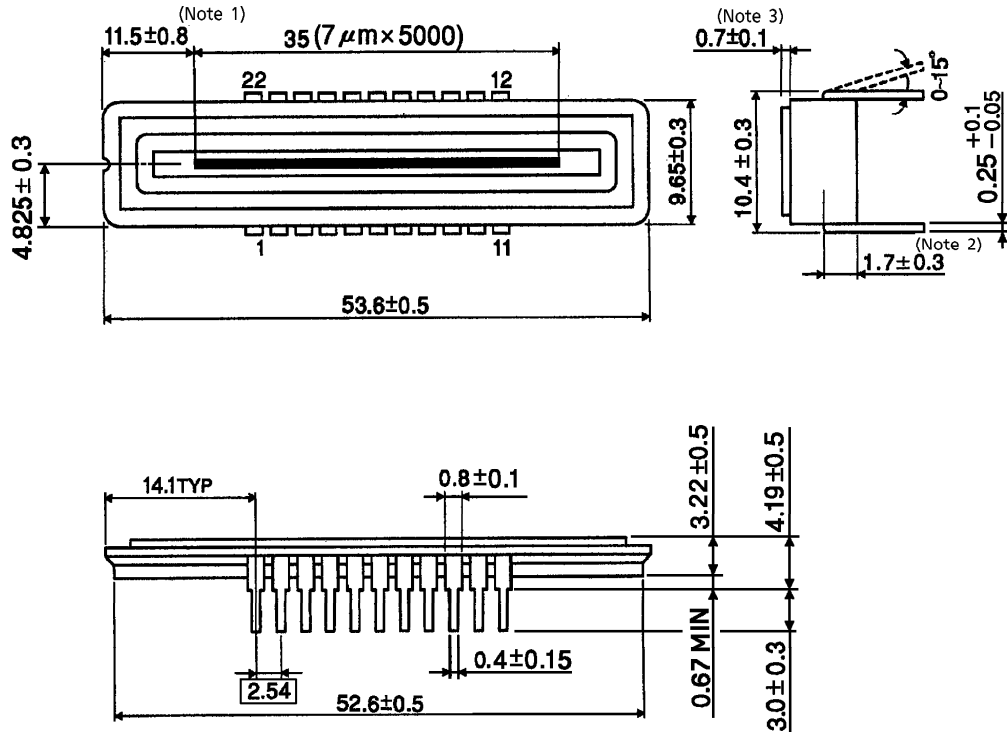
3. Incident Light

CCD image sensor has sensitivity in a wide range zone of light wave length, but its characteristics will sometimes widely change when used with long wave length input light outside the visual light zone.

PACKAGE OUTLINE

WDIP22-G-400-2.54D (B)

Unit in mm



(Note 1) : No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.

(Note 2) : TOP OF CHIP TO BOTTOM OF PACKAGE.

(Note 3) : GLASS THICKNES (n = 1.5)

Weight : 5.2 g (Typ.)